HARRIS Semiconductor

IRF244, IRF245, IRF246, IRF247

14A and 13A, 275V and 250V, 0.28 and 0.34 Ohm, N-Channel Power MOSFETs

January 1998

Features

- **14A and 13A, 275V and 250V**
- **$r_{DS(ON)}$ = 0.28Ω and 0.34Ω**
- **Single Pulse Avalanche Energy Rated**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **275V, 250V DC Rated - 120V AC Line System Operation**
- **Related Literature**
  - **TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”**

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF244	TO-204AA	IRF244
IRF245	TO-204AA	IRF245
IRF246	TO-204AA	IRF246
IRF247	TO-204AA	IRF247

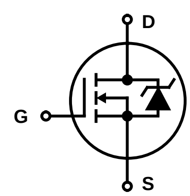
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

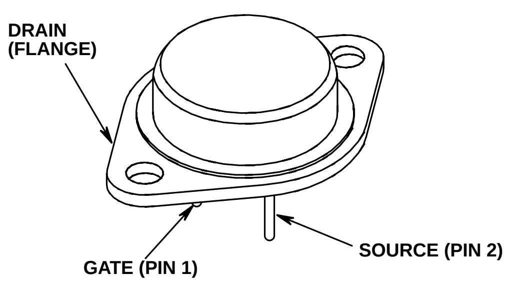
Formerly developmental type TA17423.

Symbol



Packaging

JEDEC TO-204AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRF244	IRF245	IRF246	IRF247	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	250	250	275	275	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current	ID	14	13	14	13	A
$T_C = 100^oC$	I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (Note 3)	I_{DM}	56	52	56	52	A
Gate to Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation	P_D	125	125	125	125	W
Linear Derating Factor		1.0	1.0	1.0	1.0	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	550	550	550	550	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from case for 10s	T_L	300	300	300	300	^oC
Package Body for 10s, see TB334	T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

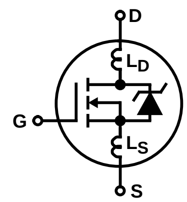
NOTE:

1. $T_J = 25^oC$ to 125^oC.

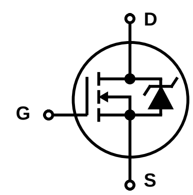
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA (Figure 10)				
IRF244, IRF245			250	-	-	V
IRF246, IRF247			275	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2.0	-	4.0	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V				
IRF244, IRF246			14	-	-	A
IRF245, IRF247			13	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On-State Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8A, (Figures 8, 9)				
IRF244, IRF246			-	0.20	0.28	Ω
IRF245, IRF247			-	0.24	0.34	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 8A, (Figure 12)	6.7	10	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D ≈ 14A, R_G = 9.1Ω, R_L = 8.9Ω (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	24	ns
Rise Time	t_r		-	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	53	80	ns
Fall Time	t_f		-	49	74	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{g(REF)}$ = 1.5mA, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	39	59	nC
Gate to Source Charge	Q_{gs}		-	6.6	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	20	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz (Figure 11)	-	1300	-	pF
Output Capacitance	C_{OSS}		-	320	-	pF
Reverse-Transfer Capacitance	C_{RSS}		-	69	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on the Flange that is Closer to Source and Gate Pins and the Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From the Flange and the Source Bonding Pad	-	12.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	1.0	$^oC/W$
Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 	-	-	14	A
Pulse Source to Drain Current (Note 3)	I_{SM}		-	-	56	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 14A, V_{GS} = 0V (Figure 13)	-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 14A, dI_{SD}/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, I_{SD} = 14A, dI_{SD}/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-On Time	t_{ON}	Intrinsic Turn-On Time is Negligible, Turn-On Speed is Substantially Controlled by $L_S + L_D$	-	-	-	-

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 50V, starting $T_J = 25^oC$, L = 4.5mH, $R_G = 25\Omega$, peak I_{AS} = 14A. See Figures 15, 16.

Typical Performance Curves Unless Otherwise Specified

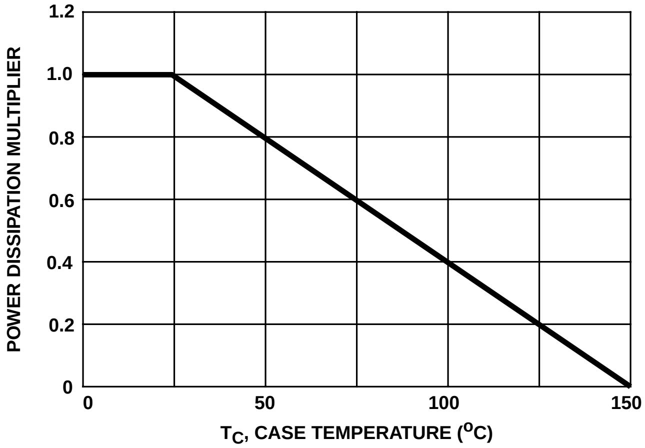


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

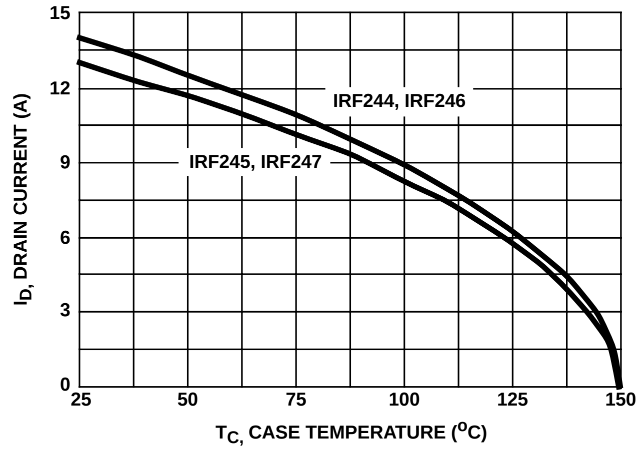


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

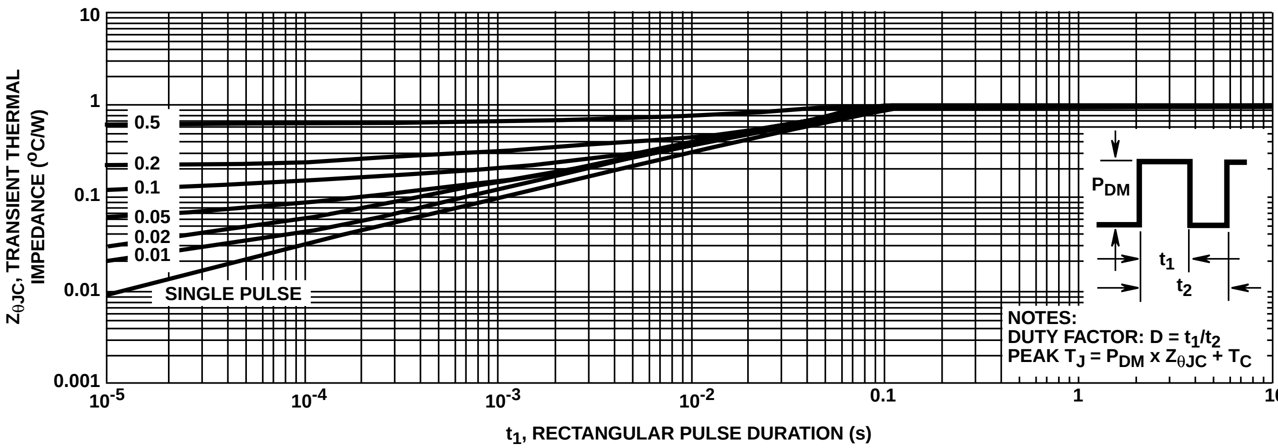


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

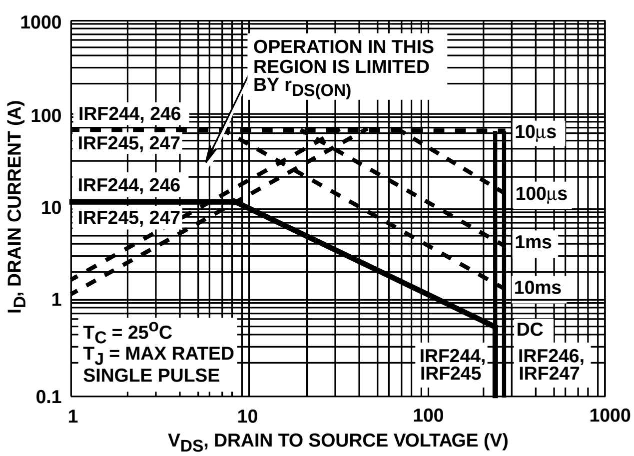


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

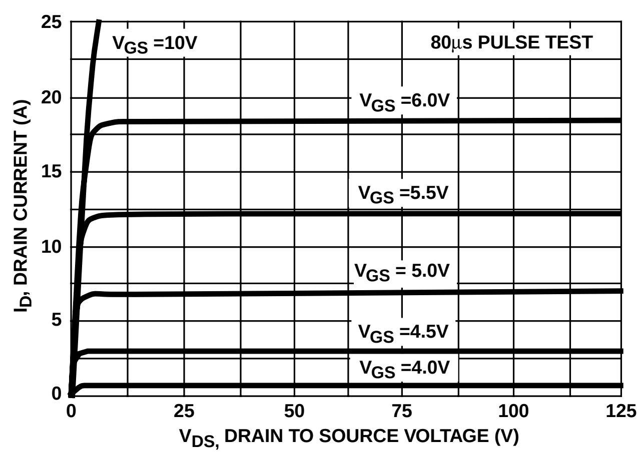


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

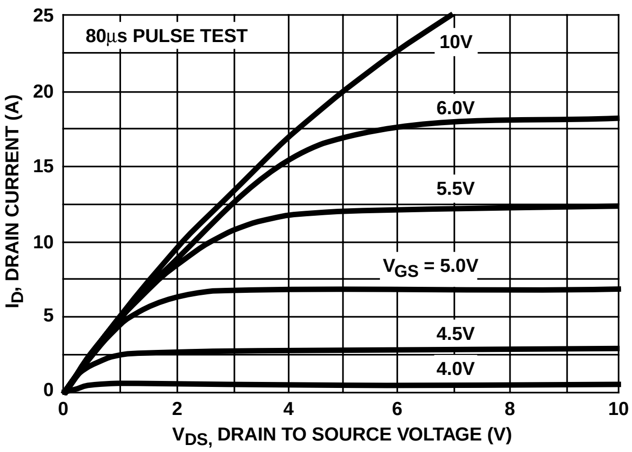


FIGURE 6. SATURATION CHARACTERISTICS

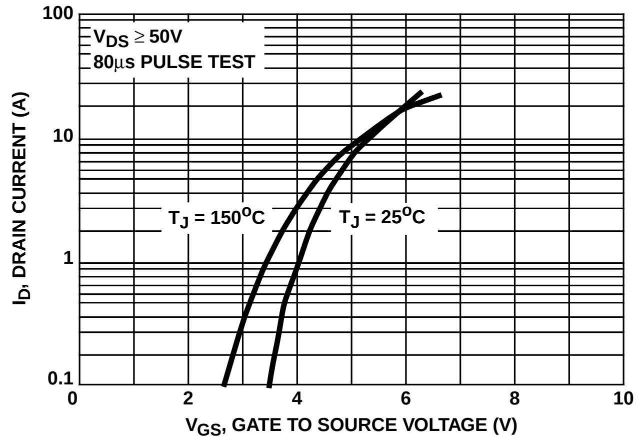


FIGURE 7. TRANSFER CHARACTERISTICS

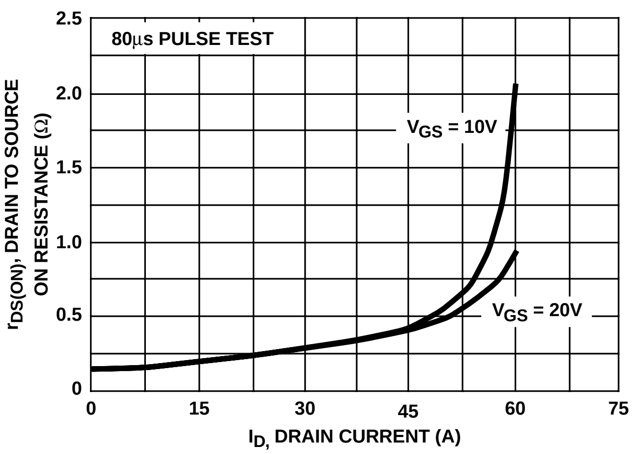


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

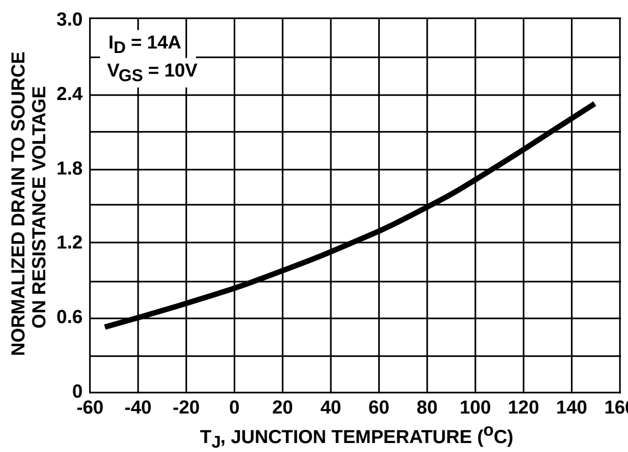


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

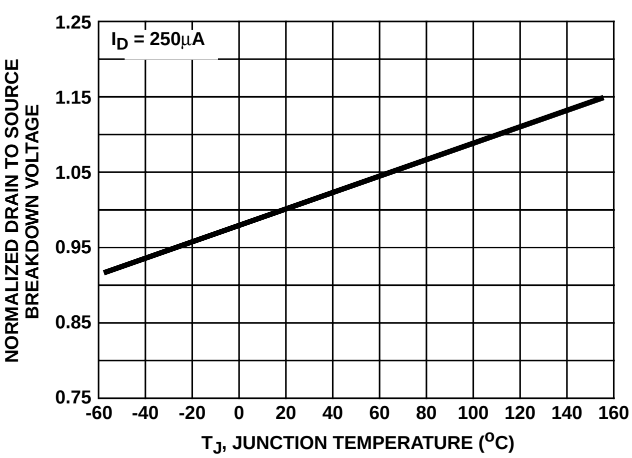


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

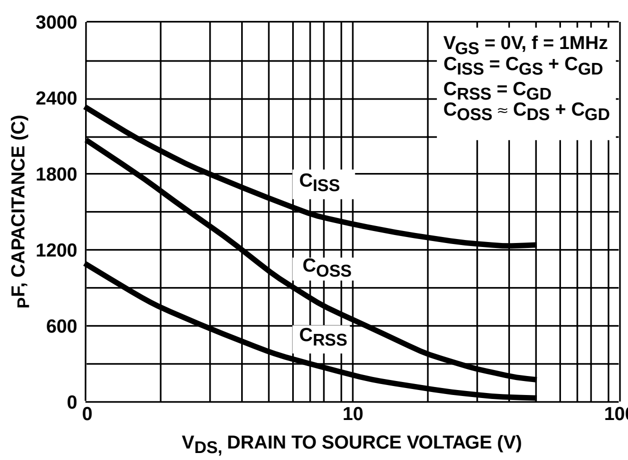


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

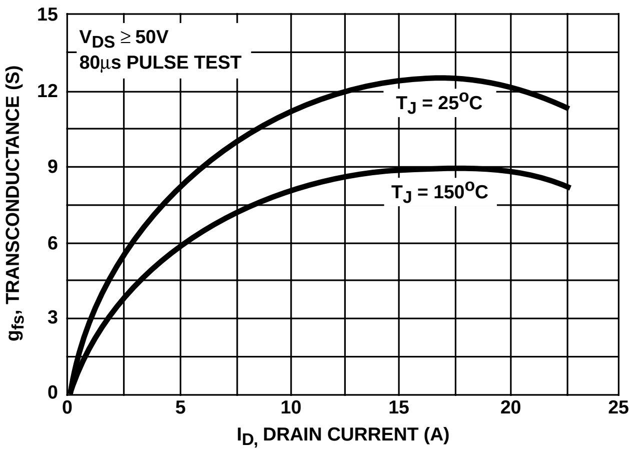


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

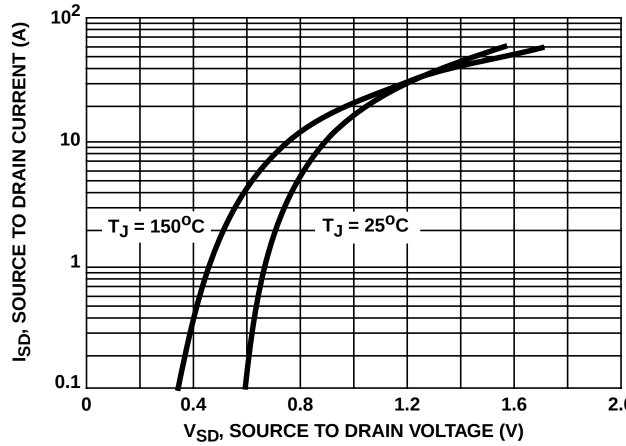


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

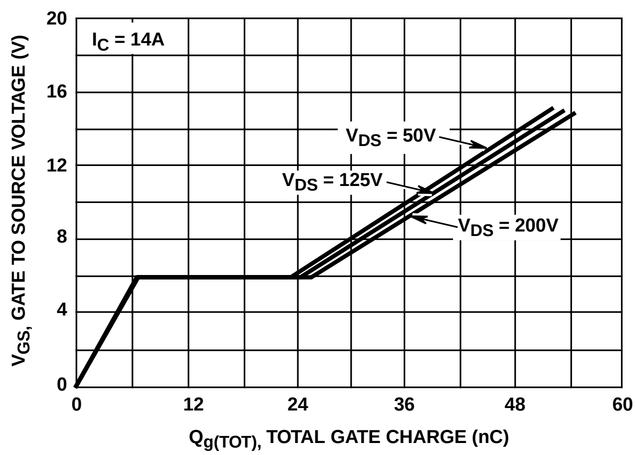


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

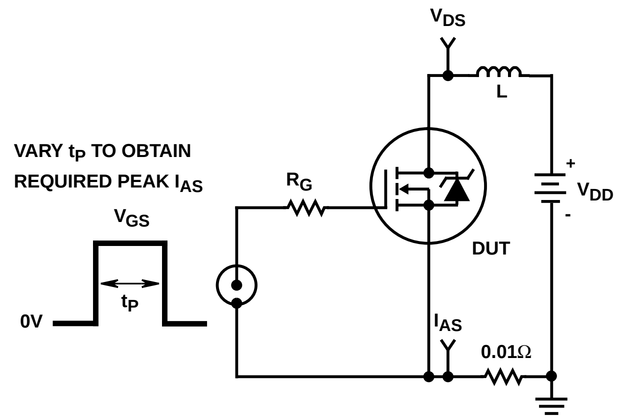


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

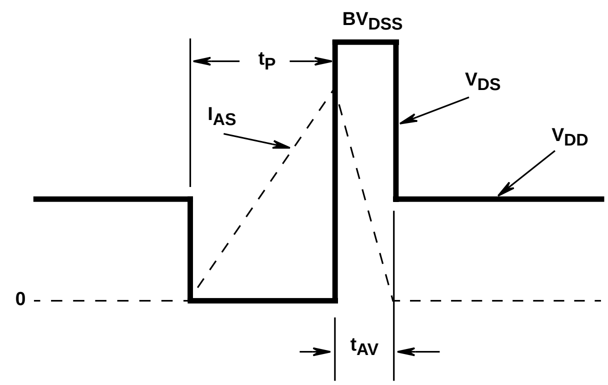


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

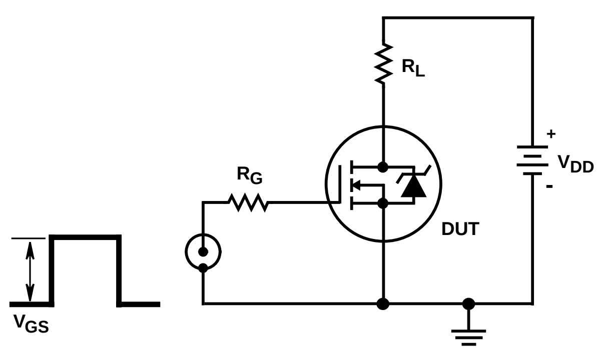


FIGURE 17. SWITCHING TIME TEST CIRCUIT

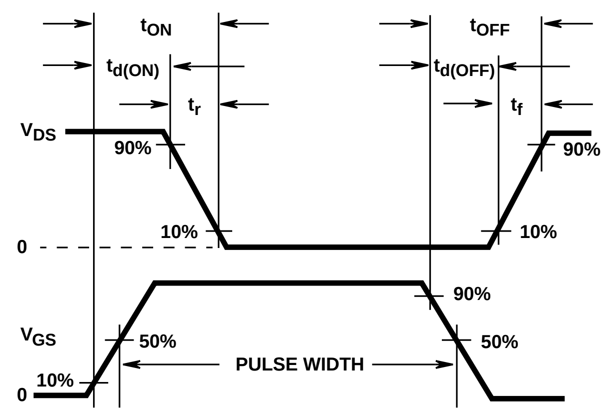


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

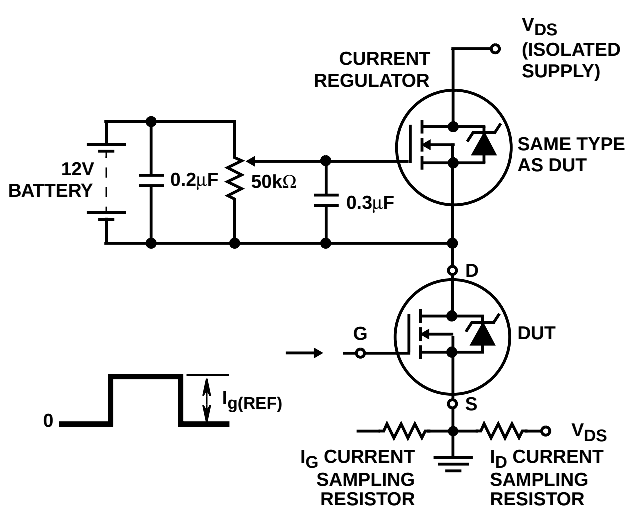


FIGURE 19. GATE CHARGE TEST CIRCUIT

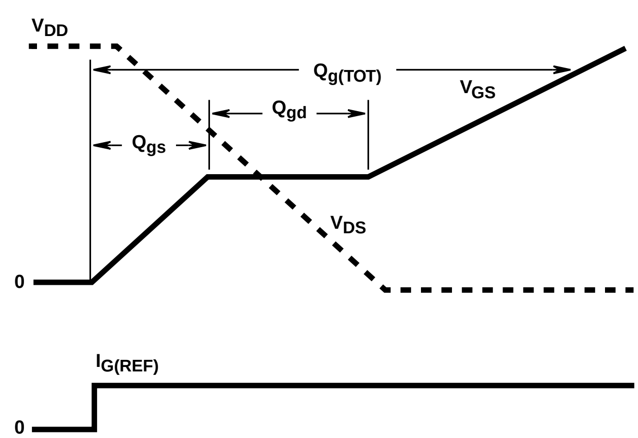


FIGURE 20. GATE CHARGE WAVEFORMS